[(Invited)] High-Performance III-V devices for future logic applications

D.-H. Kim[1,2], T.-W. Kim[1], RH. Baek[1], P. D. Kirsch[1], W. Maszara[2], J. A. del Alamo[3], D. A. Antoniadis[3], M. Urteaga[4], B. Brar[4], HM. Kwon[5], C.-S. Shin[5], W.-K. Park[5], Y.-D. Cho[6], SH. Shin[6], DH. Ko[6] and K.-S. Seo[7]

[1]SEMATECH, [2]GLOBALFOUNDRIES, [3]MIT, [4]Teledyne Scientific, [5]KANC, [6]Yonsei University and [7]Seoul National University

E-mail: Dae-Hyun.Kim@sematech.org

Abstract: High-mobility III-V transistors are poised to take the lead on future high performance logic operation. If this happens, indium-rich $In_xGa_{1-x}As$ is the most promising n-channel material. Indeed, remarkable progress has been made, including III-V gate-stacks with ALD-grown gate dielectrics. This paper reviews the evolution of high-performance III-V devices for future logic applications and discuss a possible path forward to further improve their logic figure-of-merits.

Introduction: In early 2000s, indium-rich $In_xGa_{1-x}As$ (x>0.53) has recently emerged as the most promising non-Si n-channel material for post Si CMOS logic applications [1]. This is thanks to the outstanding electron transport characteristics, excellent interfacial quality of the high-k/InGaAs gate stack by ALD and co-integration of InGaAs-based heterostructures with Si [1-2]. Recently, significant progress has been made on a variety of GaAs and InGaAs MOSFETs by many different groups. This paper reviews high-performance III-V devices for future logic applications, covers recent advances in some of the key enabling technology of InGaAs MOSFETs, and finally discusses options to further improve the performance of InGaAs MOSFETs.

How good are III-V's for future logic applications?: As a way to assess the prospects for a future III-V MOSFET technology with gate lengths in the sub-10 nm range, we started our research in 2005 on state-of-the-art III-V High-Electron-Mobility-Transistors (HEMTs). The HEMT in itself a device with near THz capabilities, was an excellent prototype Field-Effect-Transistor (FET) for future logic. The HEMT is a FET with a "medium-k" gate barrier and outstanding carrier transport properties. From 2005 to 2009, we investigated the logic characteristics of scaled-down InGaAs HEMTs [3-5]. From this time, **Figs. 1** and **2** show cross-sectional schematic and typical subthreshold/transfer characteristics of L_g = 30 nm $In_{0.7}Ga_{0.3}As$ HEMTs with t_{ins} = 4 nm at V_{DS} = 0.5 V [4-5]. DIBL, S and g_{m_max} are 120 mV/V, 90 mV/dec. and > 2.5 mS/•m at V_{DS} = 0.5 V, respectively, which outperform today's state-of-the-art Si nMOSFETs with equivalent gate length [6]. An I_{ON}/I_{OFF} ratio in excess of 10^4 in well-designed devices, even with supply voltage of 0.5 V is obtained. The device exhibits I_{ON} = ~ 0.62 mA/µm at an I_{Leak} = 100 nA/µm. This is the highest I_{ON} in any III-V FET on any material system, to date. This is about 20% higher I_{ON} than state-of-the-art high-performance 22 nm nMOSFET with comparable physical gate length and I_{Leak} at V_{DD} = 0.5 V [6]. It was data like these that showed that InGaAs-channel HEMTs prototyped in a university environment could outperformance state-of-the-art Si nMOSFETs of similar gate length at V_{DD} = 0.5 V that strongly highlighted the potential of InGaAs MOSFETs for logic.

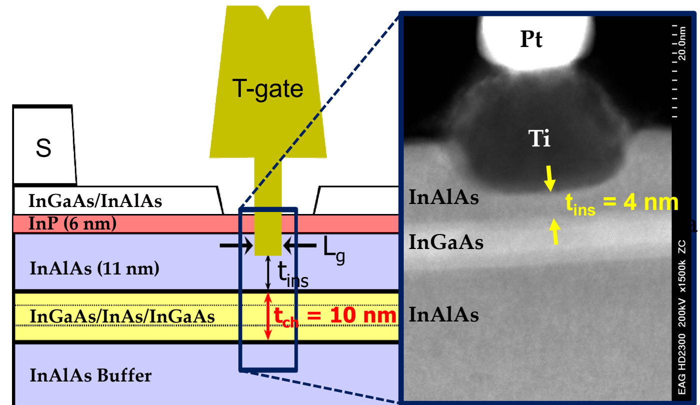


Fig. 1 Cross-sectional schematic of state-of-the-art InGaAs HEMT [4].

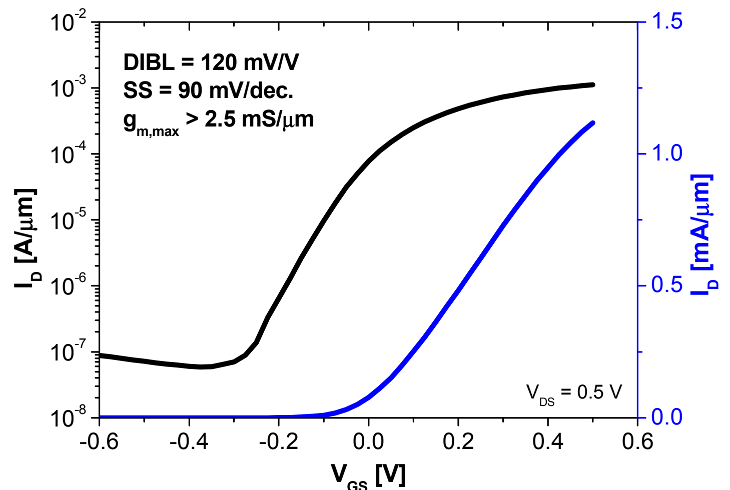


Fig. 2 Subthreshold and transfer characteristics of L_g = 30 nm InGaAs HEMT with t_{ins} = 4 nm [4-5].

Evaluation of III-V Gate Stack: The key enabling technology for InGaAs MOSFETs is a high-quality oxide/semiconductor interface by ALD. During ALD, a kind of 'self-cleaning effect' or 'clean-up effect' takes places such that III-V surface oxides are effectively removed [7]. Many different groups have demonstrated excellent Al_2O_3/InGaAs interfaces and surface-channel III-V MOSFETs. However, this is insufficient for future scaled CMOS. In particular, a dielectric with higher k is required. Also, in a surface-channel design, interface roughness scattering severely degrades the mobility (**Fig. 3**). The pressing need for the 7-nm technology node and/or beyond is for an ultra-scaled surface-channel design with total EOT well below 1 nm while maintaining excellent transport properties. We have been investigating a composite Al_2O_3/HfO_2 gate stack, where a thin Al_2O_3 interfacial layer serves as passivation. This leads to a far better mobility-EOT trade-off, while maintaining lower D_{it} on InGaAs which is confirmed by our device results (**Fig. 4**) [8].

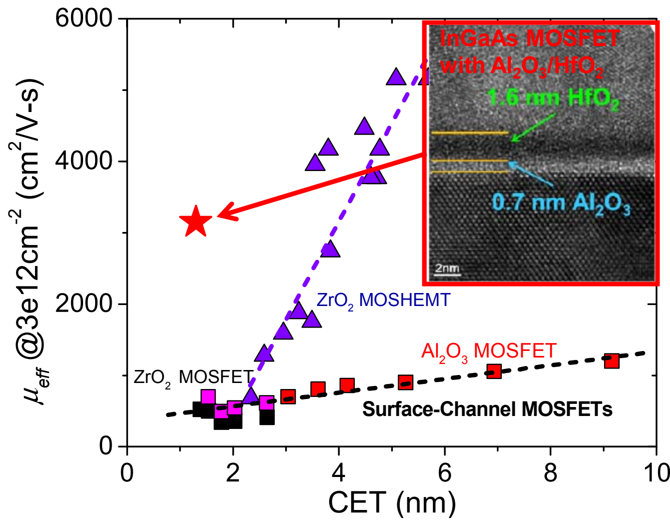


Fig. 3 μ_{eff} at $n_s = 3\times10^{12}cm^{-2}$ vs. CET for planar InGaAs QW MOSFET with Al_2O_3/HfO_2 [8] and other reports on various types of III-V MOSFETs. Inset is the cross-sectional TEM image for Al_2O_3/HfO_2 gate stack on InGaAs [8].

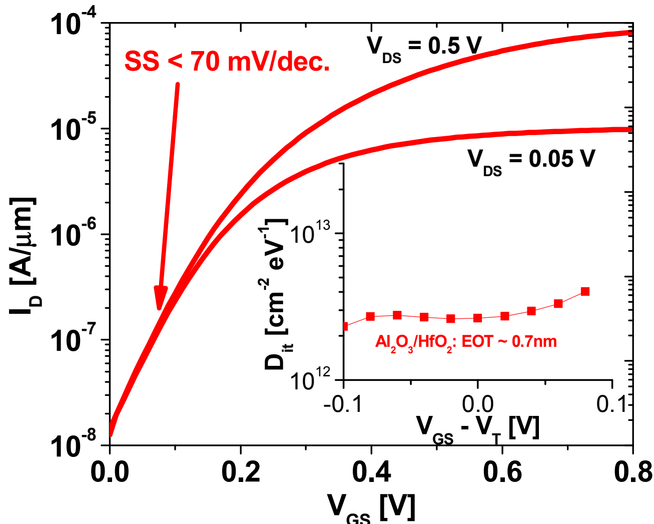
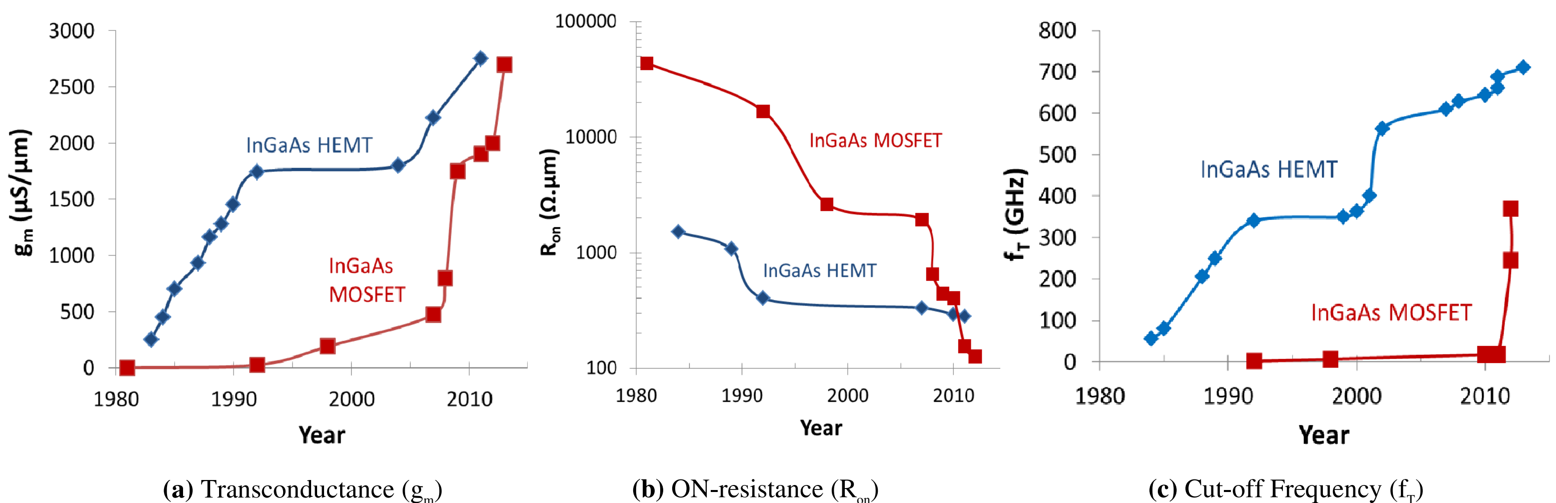


Fig. 4 Subthreshold characteristics of long-channel InGaAs MOSFET with Al_2O_3/HfO_2 at V_{DS} = 0.05/0.5 V. Inset is extracted D_{it} for Al_2O_3/HfO_2 on InGaAs channel. EOT < 1 nm, SS < 70 mV/dec., and $D_{it} \sim 2 \times 10^{12}/cm^2eV$ [8].

Progress and Prospects of InGaAs MOSFETs: Starting from III-V MOSFETs with state-of-the-art characteristics, it is very useful to benchmark InGaAs MOSFETs against InGaAs HEMTs [9]. **Figs. 5 (a), (b)** and **(c)** show the evolution of transconducntace (g_m), on-resistance (R_{on}) and the current-gain cut-off frequency (f_T) of InGaAs MOSFETs as well as InGaAs HEMTs for the last three decades. InGaAs MOSFETs have now matched the g_m of HEMTs and surpassed the R_{on} of HEMTs. The high g_m behavior in InGaAs MOSFETs stems from the ability to scale the effective oxide thickness in the MOS gate stack as well as the excellent interface-state density (D_{it}, shown in the inset of **Fig. 4**). These are also responsible for the very low R_{on}. The excellent parasitic resistance characteristics in InGaAs MOSFETs arise from the absence of an energy barrier under the S/D contracts, which is the bottleneck in InGaAs HEMTs. Recently, several groups have successfully demonstrated sub-100 nm InGaAs MOSFETs with record R_{on} and g_m behavior, approaching g_{m_max} = 3 mS/μm at V_{DS} = 0.5 V [10-12].

Figs. 6 and **7** exhibit microwave and high frequency noise-figure characteristics of an L_g = 35 nm $In_{0.7}Ga_{0.3}As$ MOSFET with Al_2O_3/HfO_2 bilayer gate stack. Excellent high-frequency characteristics can be observed in this device, such as current-gain cutoff frequency (f_T) = 440 GHz, maximum oscillation frequency (f_{max}) = 305 GHz and minimum noise-figure (NF_{min}) < 0.5 dB at 26 GHz. The results are record values for f_T and f_{max}, and the lowest NF_{min} at 26 GHz of any III-V MOSFET. It is interesting to see that today's InGaAs HEMTs still exhibit a far better f_T than InGaAs MOSFETs. This is mostly due to low-parasitic capacitance design employed in InGaAs HEMTs, such as T-gate. With the introduction of low parasitic capacitance MOSFET designs, it is expected that InGaAs MOSFETs that match or exceed the high-frequency characteristics of InGaAs HEMTs will be developed.



(a) Transconductance (g_m) **(b)** ON-resistance (R_{on}) **(c)** Cut-off Frequency (f_T)

Fig. 5 Benchmarking of Inversion-type InGaAs MOSFETs against InGaAs HEMTs, as a function of year [9].

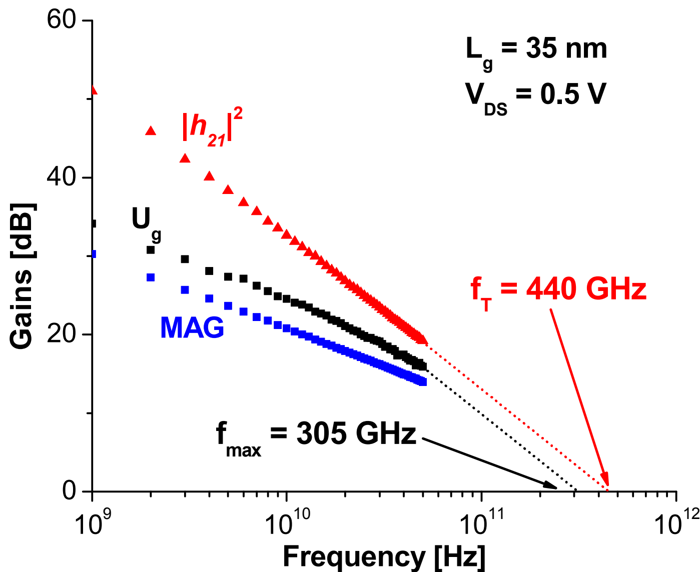


Fig. 6 RF gains (h_{21}, MAG and unilateral gain) against frequency for L_g = 35 nm $In_{0.7}Ga_{0.3}As$ MOSFETs with Al_2O_3/HfO_2 at V_{DS} = 0.5 V. The device shows a record value of f_T = 440 GHz.

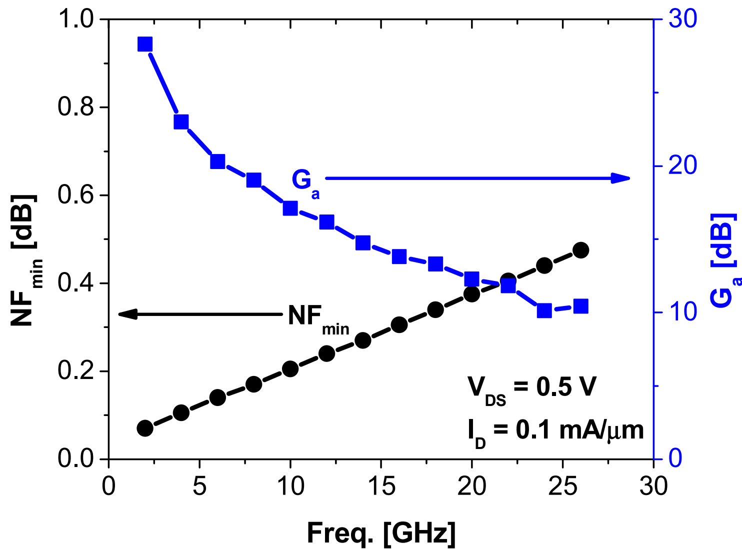


Fig. 7 High-frequency minimum noise-figure (NF_{min}) and associated gain (G_a) against frequency for L_g = 35 nm $In_{0.7}Ga_{0.3}As$ MOSFETs with Al_2O_3/HfO_2 at V_{DS} = 0.5 V.

Alternative MOSFET designs are being pursued. Epitaxial selectively-regrown S/D contacts (**Fig. 8**) have recently yielded record R_{on} and effectively mobility ($\mu_{n,eff}$) behavior in InGaAs MOSFETs [13-14]. This allows the introduction of tensile strain to boost performance [15] and enables a gate-last integration scheme that prevents degradation of the III-V gate stack [14]. Sub-10 nm MOSFETs will require 3D device architectures, such as Tri-gate FETs [16-17] or Gate-all-around FETs [18]. In Tri-gate FETs, how to define an InGaAs fin on Si is a major concern. For this, we have been investigating RIE in combination with post wet treatment. **Fig. 9** exhibits subthreshold characteristics of the state-of-the-art Tri-gate InGaAs MOSFET with $L_g/W_{fin}/H_{fin}$ = 50/30/20 nm [17]. A concern in Tri-gate MOSFETs is the sidewall MOS interface. From the subthreshold characteristics in our previous report [17], coupled with TCAD simulation, we preliminary extract D_{it} ~ 4 x 10^{12} $eV^{-1}cm^{-2}$ at the sidewall gate stack interface between Al_2O_3 and etched InGaAs fin, which is about 2 times larger than planar gate stack.

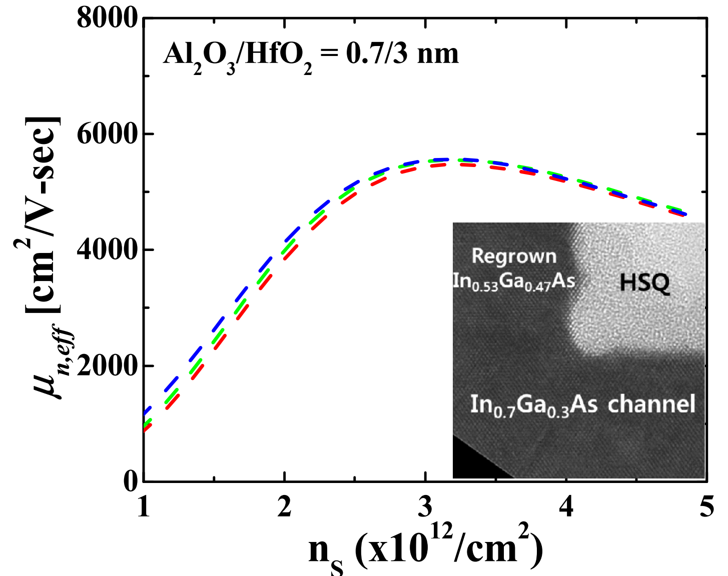


Fig. 8 Effective mobility ($\mu_{n,eff}$) as a function of carrier density (ns) for InGaAs MOSFET with epitaxial selectively-regrown S/D contact. This allows a gate-last integration scheme that prevents degradation of III-V gate-stack. This leads to a record $\mu_{n,eff}$ behavior, in excess of 5,500 cm^2/V-s at 300K [14].

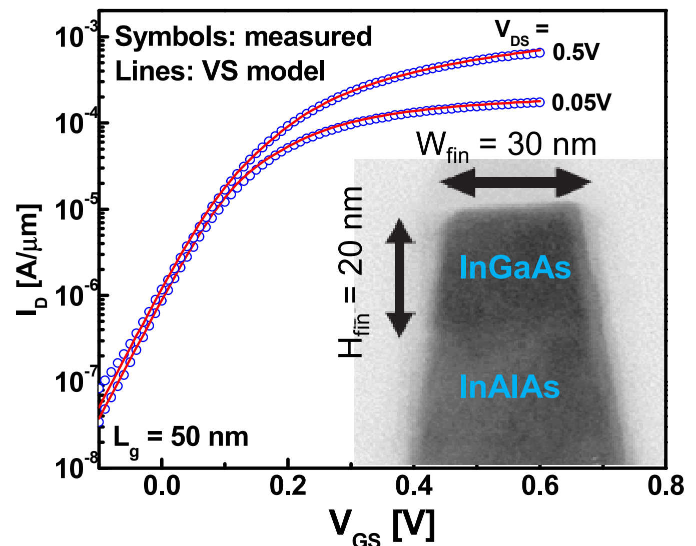


Fig. 9 Subthreshold characteristics of L_g = 50 nm InGaAs MOSFET with W_{fin}/H_{fin} = 30/20 nm. At V_{DS} = 0.5 V, the device exhibits SS < 80 mV/dec, DIBL < 20 mV/V, g_{m_max} = 1.5 mS/μm and I_{ON} = 380 mA/μm [8].

Fig. 10 highlights TCAD simulation result on the impact of D_{it} onto subthreshold-swing in double-gate (DG) InGaAs MOSFETs with L_g = 100 nm and EOT = 1 nm. Appropriate surface treatment and/or post-etch annealing process should

be explored to further improve the sidewall MOS gate stack behavior. Finally, **Fig. 11** plots benchmarking of I_{ON} against L_g for the state-of-the-art InGaAs HEMT [5] and recently published InGaAs MOSFETs. Well-designed InGaAs MOSFETs exhibit a peak g_m of 2.7 mS/μm and a record I_{ON} ~ 0.4 mA/μm at I_{OFF} = 100 nA/mm and V_{DD} = 0.5 V.

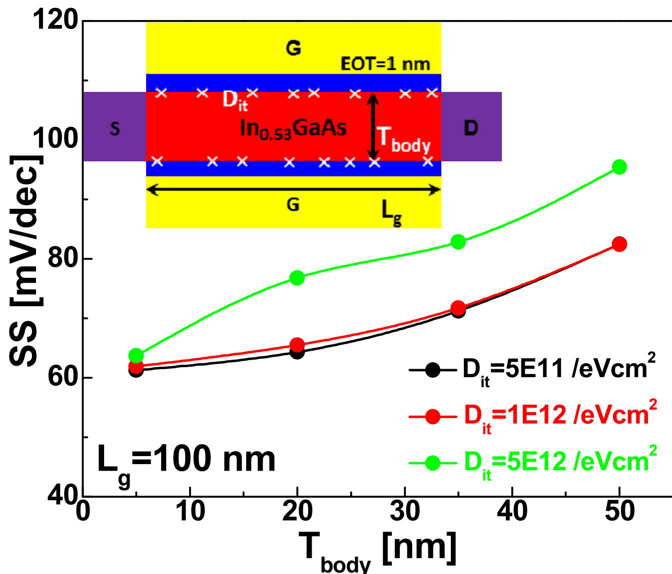


Fig. 10 Impact of D_{it} onto subthreshold-swing (SS) behavior in double-gate (DG) InGaAs MOSFETs with L_g = 100 nm and EOT = 1 nm, as a function of body thickness (T_{body}). T_{body} corresponds to fin width (W_{fin}) in tri-gate configuration.

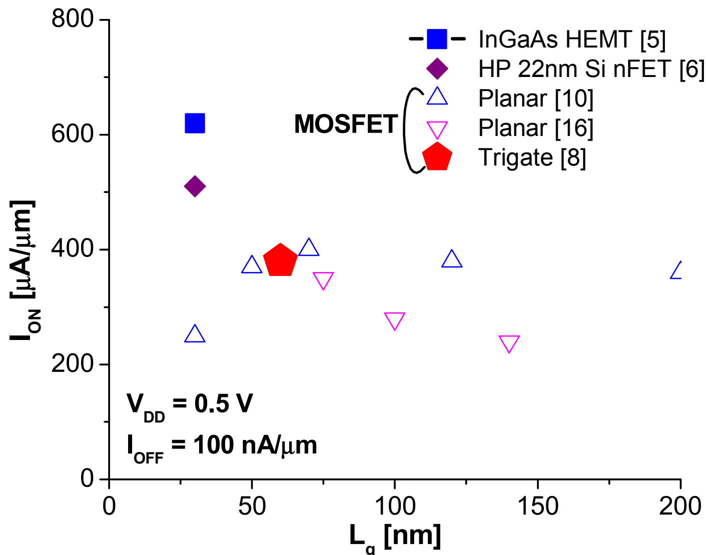


Fig. 11 Benchmarking of I_{ON} against L_g for state-of-the-art InGaAs HEMTs [5] and recent InGaAs MOSFETs with planar [10, 16] and non-planar architecture [8]. For all devices, I_{OFF} = 100 nA/mm and V_{DD} = 0.5 V.

Summary: CMOS might be about to take the disruptive step of replacing Si in the channel. If this happens, InGaAs is the most promising new channel material for n-MOSFETs. Remarkable progress has taken place, but many challenges still remain. This paper reviews high-performance III-V transistor technology for future logic applications.

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